Si$_3$N$_4$ Deposition & the Virtual Chemical Vapor Deposition Lab

Making a transistor, the general process
A closer look at chemical vapor deposition and the virtual lab

Images courtesy Silicon Run Educational Video, VCVD Lab Screenshot
On a wafer, billions of transistors are housed on a single square chip. One malfunctioning transistor could cause a chip to short-circuit, ruining the chip. Thus, the process of creating each microscopic transistor must be very precise.

Why Si₃N₄ Deposition...Making Microprocessors

Wafer image: http://upload.wikimedia.org/wikipedia/fr/thumb/2/2b/PICT0214.JPG/300px-PICT0214.JPG

http://vista.pca.org/yos/Porsche-911-Turbo.jpg

http://www.sonyericsson.com/cws/products/mobilephones/overview/x1?cc=us&lc=en
What **size** do you think an individual transistor being made today is?
Size of Transistors

One chip is made of millions or billions of transistors packed into a length and width of less than half an inch. Channel lengths in MOSFET transistors are less than a tenth of a micrometer. Human hair is approximately 100 micrometers in diameter.

Scaling of successive generations of MOSFETs into the nanoscale regime (from Intel).
Transistor: MOS

- We will illustrate the process sequence of creating a transistor with a Metal Oxide Semiconductor (MOS) transistor.

- Wafers – 12” Diameter

Image courtesy: Pro. Milo Koretsky
Chemical Engineering Department at OSU
IC Processing consists of selectively adding material (Conductor, insulator, semiconductor) to, removing it from or modifying it.

(Note that these steps are not all the steps to create a transistor. Some steps are skipped. This is purely to show the various stages in the loop to create a transistor.)
Making a Transistor:
Starting Silicon Wafer

Wafers

Deposition/Oxidation

Clean

Photo/Patterning

Etching/CMP

Ion Implant/Anneal

Si
Clean substrate

Polished Silicon Wafer

Deposition / Oxidation
Photo/Pattern Transfer
Etching / CMP
Ion Implant / Anneal

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Chemical Engineering Department at OSU
Chemical Vapor Deposition: $\text{Si}_3\text{N}_4$

Process 200 Wafers at a Time
Spin Coating of Photoresist

- Clean
- Deposition / Oxidation
- Etching / CMP
- Ion Implant / Anneal
- Photo / Pattern Transfer
- Oxide / Photo / Pattern Transfer
- Etching / CMP
- Clean

mask

Si

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Chemical Engineering Department at OSU
Develop Photoresist

- Deposition / Oxidation
- Etching / CMP
- Ion Implant / Anneal
- Clean
- Photopattern Transfer
- Loop
Plasma Etch $\text{Si}_3\text{N}_4$
Plasma Etch: Strip Photoresist

- Etching / CMP
- Ion Implant / Anneal
- Photo / Pattern Transfer
- Deposition / Oxidation
- Clean
Ion Implantation

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Chemical Engineering Department at OSU
Anneal

- Clean before anneal

Activate (& diffuse) the dopant

**HEAT**  **HEAT**  **HEAT**

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Chemical Engineering Department at OSU
The Final Steps...a completed transistor

Gate: +

Source -

Drain: +

Si

e- e-

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Chemical Engineering Department at OSU
Chemical Vapor Deposition A Closer Look: Si$_3$N$_4$

Reactions:

\[
\begin{align*}
\text{Dichlorosilane} & \rightarrow \text{Silicon nitride} \\
\text{Ammonia} & \rightarrow \text{Hydrogen chloride} \\
\text{Hydrogen} & \rightarrow \text{Ammonium chloride} \\
\end{align*}
\]

Graphics copy-write Pro. Milo Koretsky
Chemical Engineering Department at OSU
Chemical Vapor Deposition A Closer Look: Si$_3$N$_4$

Reactions:

\[
3 \text{SiCl}_2\text{H}_2 \text{(g)} + 4 \text{NH}_3 \text{(g)} \rightarrow 1 \text{Si}_3\text{N}_4 \text{(s)} + 6 \text{HCl} \text{(g)} + 6 \text{H}_2 \text{(g)}
\]

Dichlorosilane + Ammonia → Silicon nitride + Hydrogen chloride + Hydrogen

\[
\text{Si}_3\text{N}_4 \text{(s)} + 6 \text{NH}_3 \text{(g)} \rightarrow 1 \text{NH}_4\text{Cl} \text{(g)} + \text{NH}_3 \text{(gas)} + \text{DCS} \text{(gas)}
\]

Silicon nitride + Ammonia → Ammonium chloride + NH$_3$ (gas) + DCS (gas)

Overall Reaction:

\[
3 \text{SiCl}_2\text{H}_2 \text{(g)} + 10 \text{NH}_3 \text{(g)} \rightarrow \text{Si}_3\text{N}_4 \text{(s)} + 6 \text{NH}_4\text{Cl} \text{(g)} + 6 \text{H}_2 \text{(g)}
\]

Dichlorosilane (DCS) + Ammonia → Silicon nitride + Ammonium chloride + Hydrogen

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Chemical Engineering Department at OSU
What factors do you think affect the reaction and film growth?

Temperature

Reaction/Deposition Time

Concentration
Virtual CVD Overview

Choosing the Virtual CVD reactor parameters

LPCVD Console

<table>
<thead>
<tr>
<th>Temperature</th>
<th>Pressure and Flow Rates</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zone 1: 800°C</td>
<td>Pressure: 200 mTorr</td>
</tr>
<tr>
<td>Zone 2: 820°C</td>
<td>NH3 Flow: 150 sccm</td>
</tr>
<tr>
<td>Zone 3: 840°C</td>
<td>DCS Flow: 40 sccm</td>
</tr>
<tr>
<td>Zone 4: 850°C</td>
<td>Reaction Time: 122 min</td>
</tr>
<tr>
<td>Zone 5: 855°C</td>
<td></td>
</tr>
</tbody>
</table>

The reactor is ready to run with the parameters listed above. Are you sure you want to conduct a furnace run with these parameters?

Load previous parameters from run#: [ ] Load Run [ ] Start Reactor

Pressure is Fixed
Factors that Effect Reaction and Film Growth: Concentration

- Absolute flow rates of NH₃ to SiCl₂H₂
- Ratio of NH₃ to SiCl₂H₂
- Pressure (fixed)

\[ PV = nRT \]
Factors that Effect Reaction and Film Growth: Temperature

- There are 5 temperature zones
- Remember (18.12, Addison-Wesley, Chemistry)

Rate = $k[A]^1$

$$k = k_0 \exp\left(-\frac{E_{a,f}}{RT}\right)$$

The Arrhenius Equation

First order reaction (thermal):

Energy

Reaction coordinate

$A \rightarrow B$
Factors that Effect Reaction and Film Growth:

Temperature

● What can you do with the 5 temperature zones???

\[ PV = nRT \]
Factors that Effect Reaction and Film Growth: Deposition Time aka Reaction Time

- Reaction/Deposition Time = the amount of time the reactor runs
- How do you think deposition time effects the film thickness???
Virtual CVD Overview

Choosing the Virtual CVD reactor parameters

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Each run costs $
Film thickness is determined by the amount of material that reacts and is grown on the wafer.

Uniformity describes the evenness of film thickness on the wafer.

**45% Uniformity**

**100% Uniformity**
Film thickness is determined by the amount of material that reacts and is grown on the wafer.

Uniformity describes the evenness of film thickness on the wafer.

Measurement – Thickness & Uniformity

SiCl$_2$H$_2$ (gas) → NH$_4$Cl (gas) → NH$_3$ (gas) → SiCl$_2$H$_2$ (gas)

79% Overall Efficiency

50% Overall Efficiency
The ellipsometer is used to measure the thickness and refractive index of transparent films. It is made of a light source and polarizer on one side and a analyzer and detector on the other side.

- Light from the source is polarized and reflected off the film.
- The analyzer is rotated till no light passes through it.
- The angle of rotation depends on the thickness of the film.
Virtual CVD Overview

Choosing the locations on the wafer to measure

Ellipsometer Console

Click on the wafer below to choose measurement coordinates.

Each measurement costs $
Virtual Chemical Vapor Deposition (VCVD) Program

VCVD Program

Semiconductor Manufacturing Fab

Photo Courtesy of http://webmedia.national.com/gallery/06/06_rgb.jpg
Your Objectives:

- Determine how temperature, flow rates, and reaction time impact deposition of Si₃N₄
- Minimize cost of testing process used to determine the impact of these parameters
- Extra Credit: Find an optimized “recipe” that produces high uniformity (within wafer and between wafers) and meets a target thickness of 1000 Angstroms
Economy of Transistors

~$300 /chip
X ~200 chips/wafer
X 200 wafers/furnace
load =

$12 Million
per furnace load

http://www.dvhardware.net/article16696.html
http://www.nitride.co.jp/english/products/wafer.html
Let’s Get Started

- Open VCVD Program...

Virtual Fab Lab

Username: student
Password: ****
Login  Quit